SQ7515 Brief Datasheet
V1.0

Content

1. Product Overview

1.1 Features

- **Basic Information**
  - Operating voltage: 2.0V ~ 3.6V
  - Operating temperature: -40°C ~ 85°C
  - Max system frequency: 24 MHz
  - Instruction set is compatible with Toshiba TLCS-870/C1
- **Memory Configuration**
  - 64 KB Flash
  - 4 KB RAM
- **Power Consumption**
  - Normal mode: 190 uA/MHz @ 3.3V (Security Processor is disable)
  - Deep Sleep mode: 1.9 uA @ 3.3V (RTC enable, CPU and RAM are retained)
- **Clock Sources**
  - External High Frequency Crystal :1~16 MHz
  - External Low Frequency Crystal :32 kHz
  - PLL
  - Internal High Frequency Oscillator : 16MHz
  - Internal Low Frequency Oscillator : 32 kHz
- **I/O**
  - 39 I/Os
  - 3sets UART, 1 set I2C, 2 sets SIO
- **Multiplier and Dividor**
  - 16 x16-bit , multiplication and 32-bit addition
  - 32-bit divid 32-bit
- **External Interrupt**
  - 8 external interrupt input (EINT0~EINT7)
- **Timer/Counter**
  - Eight 16-bit timer/counter, with timer mode, external trigger mode, pulse width measurement mode, PPG mode
  - Real-time clock (RTC)
  - Watchdog timer (WDT)
- **12-bit ADC**
  - 12CH ADC input
  - ADC Vref
- **Low Voltage Detect (LVD)**
  - 2.35V/2.65V/2.85V/3.15V
- **BROR**
  - 1.9V/2.25V/2.55V/2.75V
- **Security Processor**
  - TRNG
  - SHA-256
  - AES-128/256
  - 256 Bytes Secure User Zone
  - 768 Bytes Secure Small Zone
- **128-bit UID (Unique ID)**
- **Cyclic Redundancy Check (CRC)**
- **Data Integrity Check (DIC)**
- **Package Type**
  - QFP 10x10 44 pin
- **Applications**
  - Home Appliance
  - Consumer Electronics
  - Program Protection

1.2 Outline of Function

Product No.	SQ7515QA044SETR
Pins/ IOs	44 (39)
Operating Voltage	2.0~3.6V
Operating Temp.	-40~85C
External Interrupt	8
Flash	64K Bytes
RAM	4K Bytes
Security Processor	256 Bytes Secure User Zone 768 Bytes Secure Small Zone TRNG,SHA-256, AES-128/256,
ADC	12-bit x 12-CH (VDD, external)
Interrupt	External: 8 Internal: 28
Internal Oscillator / Accuracy	16MHz +/- 1% @ 0~50C +/- 1.5% @ -20~70C +/- 3% @ -40~85C
External Crystal	1~16MHz or 32768Hz
BROR	4 Levels
LVD	4 Levels (+/- 3%)*2
Timer / Counter	16-bit x 8
	WDT,TBT,RTC
PWM/PPG	16-bit x 8
Communication	UART x 3, SIO x 2, I2C x 1
OCDE	Yes
Pacakge Type	QFP44

Note 1: " VDD" means using VDD as internal reference voltage; "external" means there is on external reference voltage.
Note 2: Detail accuracy please refer to " 3.6 LVD characteristics.

1.3 Block Diagram

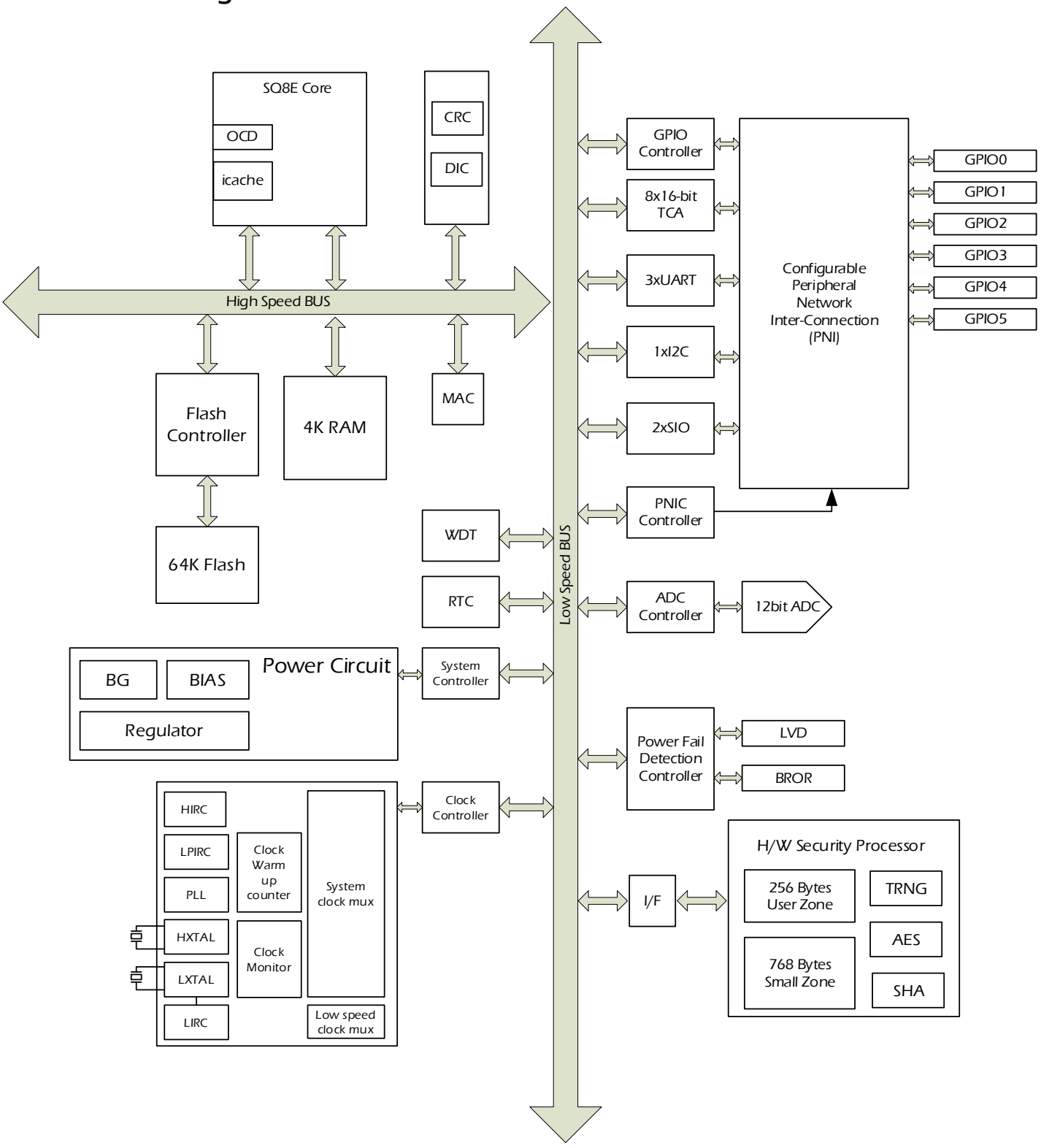


FIGURE 1- 1 BLOCK DIAGRAM

1.4 Pin Assignment/Description

QFP44 (10x10) - SQ7515QA044SETR

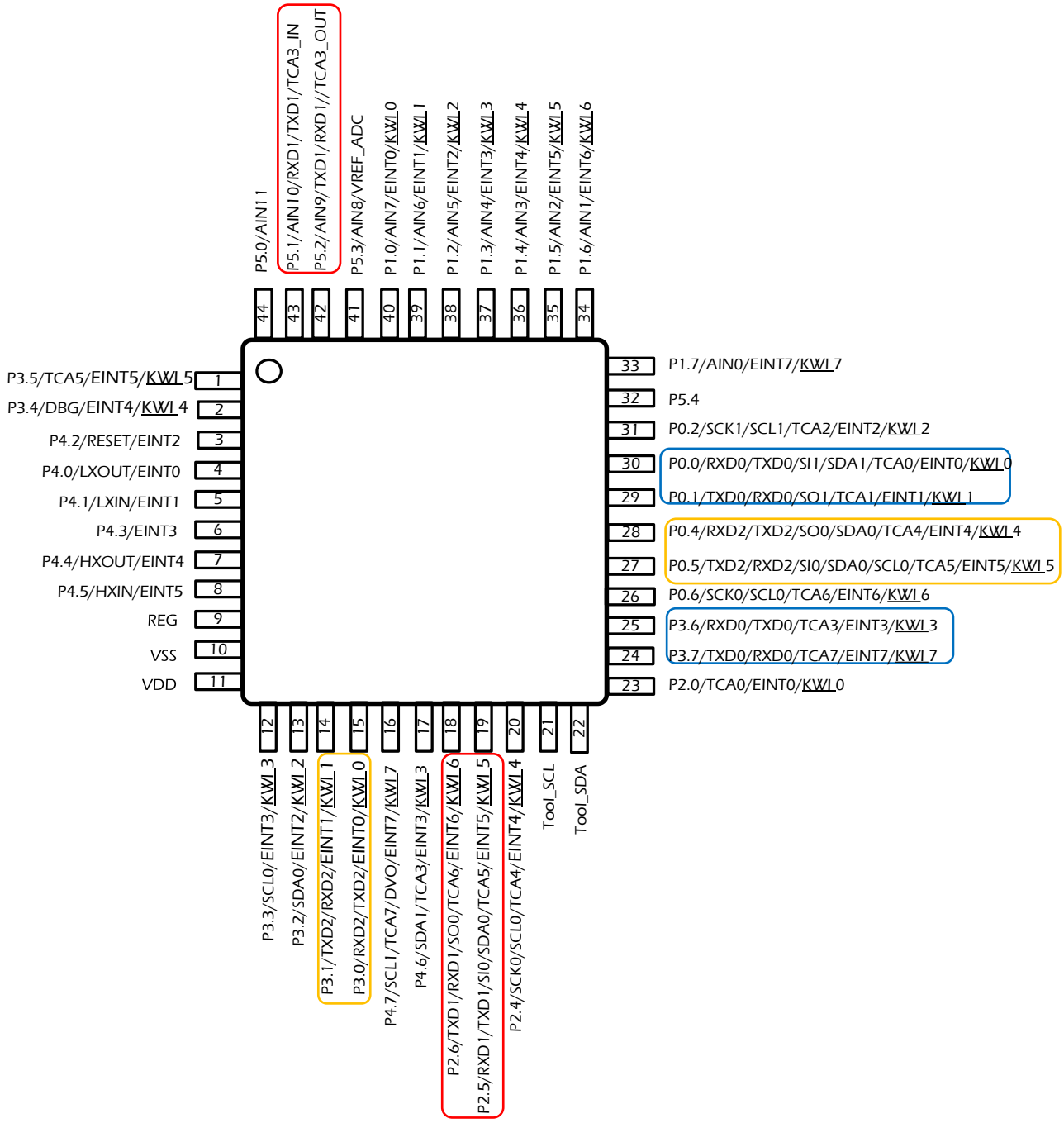


FIGURE 1- 2 PIN ASSIGNMENT OF SQ7515

Note 1：Tool_SCL, Tool_SDA are the communiation ports to the tool. Please reserve these pins in the system board. And add external pull-up resistor 4.7 kΩ to Tool_SCL, Tool_SDA separately.

Note 2：The emulation pins are P3.4/DBG, P4.2/RESET, VDD, GND. Please reserve the emulation pins in the system board. Please refer to the recommended external application circuits, other components added may affect performance or functions.

Note 3：SQ7515 can be programming (by writer) by 4-wire OCDE. Suggest to reserve the programming pins in the system board. Please refer to recommended external application circuits, other components added may affect progamming performance or functions. The 4-wire OCDE pins are same as emulation pins (P3.4/DBG,P4.2/RESET, VDD, VSS). The OCDE programming time for 64Kbyte memory is around 9 seconds.

Note 4：TCAx supports timer input/ output. P5.1/TCA3_IN supports only timer timer input, and P5.2/TCA3_OUT supports only timer timer output.

Note 5：UART / I2C/ SIO pins need to be paired as below. For example : if select P0.0 as RXD0, and P0.1 has to be TXD0.

UART0	TXD0/RXD0	P0.0/RXD0/TXD0 P0.1/TXD0/RXD0	P3.6/RXD0/TXD0 P3.7/TXD0/RXD0
UART1	TXD1/RXD1	P2.5/RXD1/TXD1 P2.6/TXD1/RXD1	P5.1/RXD1/TXD1 P5.2/TXD1/RXD1
UART2	TXD2/RXD2	P0.4/RXD2/TXD2 P0.5/TXD2/RXD2	P3.0/RXD2/TXD2 P3.1/TXD2/RXD2

I2C0	SCL0/SDA0	P0.6/SCL0 P0.5/SDA0	P0.5/SCL0 P0.4/SDA0	P2.4/SCL0 P2.5/SDA0	P3.3/SCL0 P3.2/SDA0

SIO0	SCK0/ SI0/ SO0	P0.6/SCK0 P0.5/SI0 P0.4/SO0	P2.4/SCLK0 P2.5/SI0 P2.6/ SO0
SIO1	SCK1/SI1 / SO1	P0.2/SCLK1 P0.0/SI1 P0.1/SO1	

Note 6：I/O, wake up pin and external interrupt table as below：

Pin Name					Pin/Port function	
					Key-on Wakeup	External Interrupt
P0.0	P1.0	P2.0	P3.0		KWI 0	EINT0
P0.1	P1.1	-	P3.1		KWI 1	EINT1
P0.2	P1.2	-	P3.2		KWI 2	EINT2
-	P1.3	-	P3.3 P3.6	P4.6	KWI 3	EINT3
P0.4	P1.4	P2.4	P3.4		KWI 4	EINT4
P0.5	P1.5	P2.5	P3.5		KWI 5	EINT5
P0.6	P1.6	P2.6	-	-	KWI 6	EINT6
-	P1.7	-	P3.7	P4.7	KWI 7	EINT7
				P4.0		EINT0
				P4.1		EINT1
				P4.2		EINT2
				P4.3		EINT3
				P4.4		EINT4
				P4.5		EINT5

44 Pin No.	Pin Name/ Pin Option	I/O Type	Function Description
1	P3.5/ TCA5/EINT5/KWI5	I/O (Type A)	P3.5 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. 16-bit timer pin TCA5 , external interrupt EINT5, and wake up pin KWI5 are pin-shared with P3.5.
2	P3.4/ DBG/EINT4/KWI4	I/O (Type A)	P3.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. OCDE pin DBG , external interrupt EINT4, and wake up pin KWI4 are pin-shared with P3.4.
3	P4.2/RESET/EINT2	I/O (Type A)	P4.2 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. RESET and external interrupt EINT2 are pin-shared with P4.2. RESET is low-active
4	P4.0/LXOUT/EINT0	I/O (Type B)	P4.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. LXOUT and external interrupt EINT0 are pin-shared with P4.0. LXOUT is connected to a low frequency external crystal for system clock.
5	P4.1/LXIN/EINT1	I/O (Type B)	P4.1 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. LXIN and external interrupt EINT1 are pin-shared with P4.1. LXIN is connected to a low frequency external crystal for system clock.
6	P4.3/EINT3	I/O (Type A)	P4.3 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. External interrupt EINT3 is pin-shared with P4.3
7	P4.4/HXOUT/EINT4	I/O (Type B)	P4.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. HXOUT and external interrupt EINT4 are pin-shared with P4.4. HXOUT is connected to a high frequency external crystal for system clock.
8	P4.5/HXIN/EINT5	I/O (Type B)	P4.5 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. HXIN is connected to a high frequency external crystal for system clock.
9	REG	(Type C)	Note：REG pin cannot supply to external circuit.
10	VSS	GND	Ground
11	VDD	Power	Positive power supply.
12	P3.3/SCL0/EINT3/KWI3	I/O (TypeA)	P3.3 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SCL0(I2C bus clock input/output 0) , external interrupt EINT3, and wake up pin KWI3 are pin-shared with P3.3

44 Pin No.	Pin Name/ Pin Option	I/O Type	Function Description
13	P3.2/SDA0/EINT2/KWI2	I/O (Type A)	P3.2 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SDA0 (I2C bus data input/output 0) , external interrupt EINT2, and wake up pin KWI2 are pin-shared with P3.2
14	P3.1/TXD2/RXD2/ EINT1/KWI1	I/O (Type A)	P3.1 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART TXD2/RXD2 , external interrupt EINT1, and wake up pin KWI1 are pin shared with P3.1.
15	P3.0/RXD2/TXD2/ EINT0/KWI0	I/O (Type A)	P3.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART RXD2/TXD2 , external interrupt EINT0, and wake up pin KWI0 are pin shared with P3.0.
16	P4.7/TCA7 /DVO/ EINT7 /KWI7	I/O (Type A)	P4.7 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SCL1(I2C bus clock input/output 0), 16-bit timer pin TCA7 ,DVO , external interrupt EINT7, and wake up pin KWI7 are pin-shared with P4.7.
17	P4.6/TCA3/ EINT3 /KWI3	I/O (Type A)	P4.6 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SDA1 (I2C bus data input/output 0) , 16-bit timer pin TCA3 , external interrupt EINT3, and wake up pin KWI 3 are pinshared with P4.6.
18	P2.6/TXD1/RXD1/SO0/TCA6/ EINT6 /KWI6	I/O (Type A)	P2.6 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART TXD1/RXD1 , SO0 (serial data output 0) , 16-bit timer pin TCA6 , external interrupt EINT6, and wake up pin KWI6 are pin-shared with P2.6.
19	P2.5/RXD1/TXD1/SI0/SDA0/TCA5/ EINT5 /KWI5	I/O (Type A)	P2.5 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART RXD1/TXD1, SI0(serial data input 0), SDA0 (I2C bus data input/output 0),16-bit timer pin TCA5, external interrupt EINT5, and wake up pin KWI5 are pin-shared P2.5.
20	P2.4/SCK0/SCL0/TCA4 / EINT4 /KWI4	I/O (Type A)	P2.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SCK0 (Serial clock input/output 0), SCL0(I2C bus clock input/output 0), 16-bit timer pin TCA4 , external interrupt EINT4, and wake up pin KWI4 are pin-shared P2.4.
21	Tool_SCL	-	Tool_SCL is the communiation port to the tool. Please add external pull-up resistor 4.7 kΩ to pin21.
22	Tool_SDA	-	Tool_SDA is the communiation port to the tool. Please add external pull-up resistor 4.7 kΩ to pin22.

44 Pin No.	Pin Name/ Pin Option	I/O Type	Function Description
23	P2.0/ TCA0/ EINT0 /KWI0	I/O (Type A)	P2.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. 16-bit timer pin TCA0 , external interrupt EINT0, and wake up pin KWI 0 are pin-shared with P2.0.
24	P3.7/TXD0/RXD0/TCA7/ EINT7 /KWI7	I/O (Type A)	P3.7 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART TXD0/RXD0 , 16-bit timer pin TCA7 , external interrupt EINT7, and wake up pin KWI7 are pin-shared with P3.7
25	P3.6/RXD0/TXD0/TCA3/ EINT3 /KWI3	I/O (Type A)	P3.6 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART RXD0/TXD0 , 16-bit timer pin TCA3, external interrupt EINT3, and wake up pin KWI3 are pin-shared with P3.6
26	P0.6/SCK0/SCL0/TCA6/ EINT6 /KWI6	I/O (Type A)	P0.6 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SCK0 (Serial clock input/output 0), SCL0(I2C bus clock input/output 0) ,16-bit timer pin TCA6, external interrupt EINT6, and wake up pin KWI6 are pin-shared P0.6.
27	P0.5/TXD2/RXD2/SI0/SDA0/SCL0/TCA5/ EINT5 /KWI5	I/O (Type A)	P0.5 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART TXD2/RXD2 , SI0(serial data input 0), SDA0 (I2C bus data input/output 0) , SCL0(I2C bus clock input/output 0), 16-bit timer pin TCA5, external interrupt EINT5, and wake up pin KWI5 are pin-shared with P0.5.
28	P0.4/RXD2/TXD2/SO0/SDA0/TCA4/ EINT4 /KWI4	I/O (Type A)	P0.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART RXD2/TXD2, SO0 (serial data output 0) SDA0 (I2C bus data input/output 0) , 16-bit timer pin TCA4, external interrupt EINT4, and wake up pin KWI4 are pin-shared with P0.4
29	P0.1/TXD0/RXD0/SO1/TCA1 / EINT1 /KWI1	I/O (Type A)	P0.1 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART TXD0/RXD0 , SO1 (serial data output 1), 16-bit timer pin TCA1 ,external interrupt EINT1, wake up pin KWI1, and ISPTxD/ ISPSO are pin-shared with P0.1
30	P0.0/RXD0/TXD0/SI1/ TCA0/EINT0 /KWI0	I/O (Type A)	P0.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. UART RXD0/TXD0, SI1 (serial data input 1), SDA1 (I2C bus data input/output 1) , 16-bit timer pin TCA0, external interrupt EINT0, and wake up pin KWI0, are pinshared with P0.0
31	P0.2/ SCLK1/ TCA2/EINT2 /KWI2	I/O (Type A)	P0.2 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. SCK1 (Serial clock input/output 1), SCL1(I2C bus clock input/output 1) ,16-bit timer pin TCA2 , external interrupt EINT2, and wake up pin KWI2, are pin-shared with P0.2.

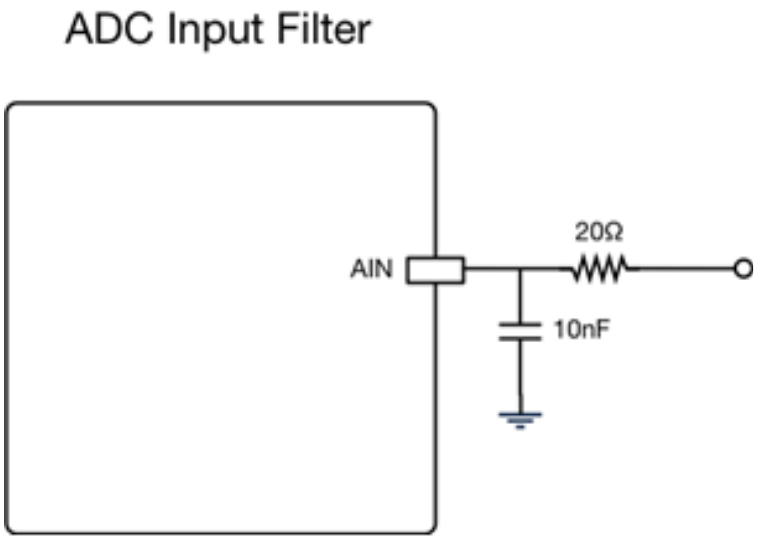
44 Pin No.	Pin Name/ Pin Option	I/O Type	Function Description
32	P5.4	I/O (Type A)	P5.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors.
33	P1.7/AIN0/EINT7 /KWI7	I/O (Type D)	P1.7 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN0, external interrupt EINT7, wake up pin KWI 7, are pin-shared with P1.7
34	P1.6/AIN1/EINT6 /KWI6	I/O (Type D)	P1.6 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN1, external interrupt EINT6, and wake up pin KWI 6, are pin-shared with P1.6.
35	P1.5/AIN2/EINT5 /KWI5	I/O (Type D)	P1.5 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN2 , external interrupt EINT5, and wake up pin KWI 5 are pin-shared with P1.5.
36	P1.4/AIN3/EINT4 /KWI4	I/O (Type D)	P1.4 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN3 , external interrupt EINT4, and wake up pin KWI 4 are pin-shared with P1.4.
37	P1.3/AIN4/EINT3 /KWI3	I/O (Type D)	P1.3 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN4 , external interrupt EINT3, and wake up pin KWI3 are pin-shared with P1.3.
38	P1.2/AIN5/EINT2 /KWI2	I/O (Type D)	P1.2 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN5, external interrupt EINT2, and wake up pin KWI2 are pin-shared with P1.2.
39	P1.1/AIN6/EINT1 /KWI1	I/O (Type D)	P1.1 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN6 , external interrupt EINT1, and wake up pin KWI1 are pin-shared with P1.1.
40	P1.0/AIN7/EINT0 /KWI0	I/O (Type D)	P1.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN7, external interrupt EINT0, and wake up pin KWI0 are pin-shared with P1.0.
41	P5.3/AIN8/VREF_ ADC	I/O (Type D)	P5.3 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN8 and VREF_ADC is pin-shared with P5.3
42	P5.2/AIN9/TXD1/RXD1/TCA3_ OUT	I/O (Type D)	P5.2 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN9, UART TXD1/RXD1 ,and 16-bit timer pin TCA3_OUT are pin-shared with P5.2.
43	P5.1/AIN10/RXD1/TXD1/TCA3 _IN	I/O (Type D)	P5.1 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN10, UART TXD1/RXD1 ,and 16-bit timer pin TCA3_IN are pin-shared with P5.1.

44 Pin No.	Pin Name/ Pin Option	I/O Type	Function Description
44	P5.0/AIN11	I/O (Type D)	P5.0 is bi-directional I/O pin, which are software configurable to be with pull-up or pull-down resistors. ADC input AIN11 is pin-shared with P5.0.

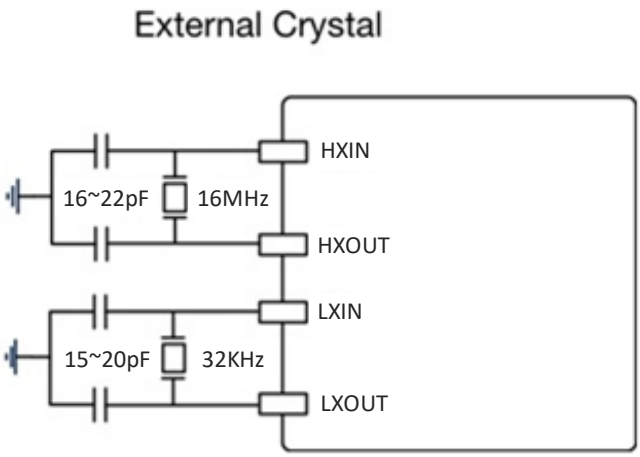
Note 1：For emulation, user has to connect to P3.4/DBG, P4.2/RESET, VDD, GND.

Recommended external application circuits are below figures, please follow the recommendation to design：

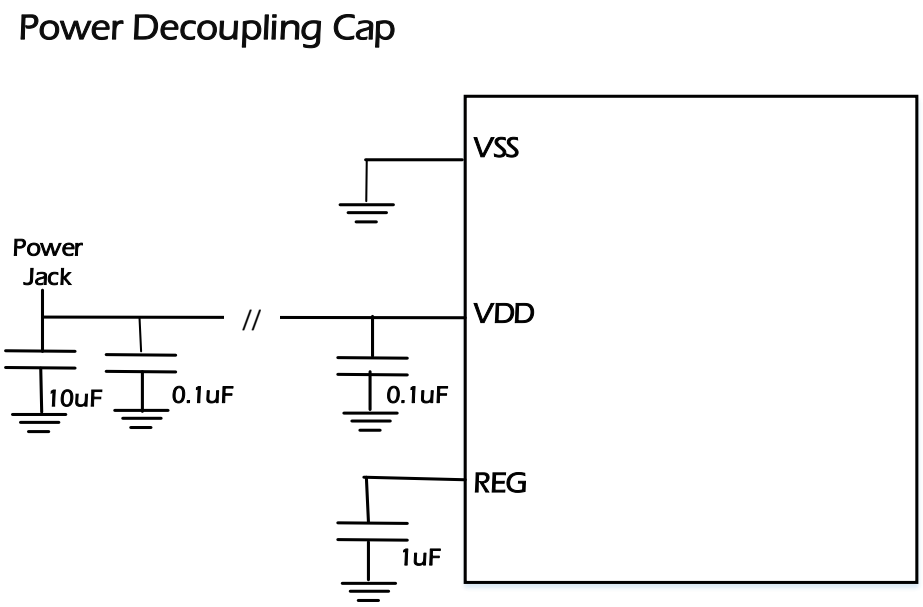
1. ADC Input Filter：



2. External Crystal：

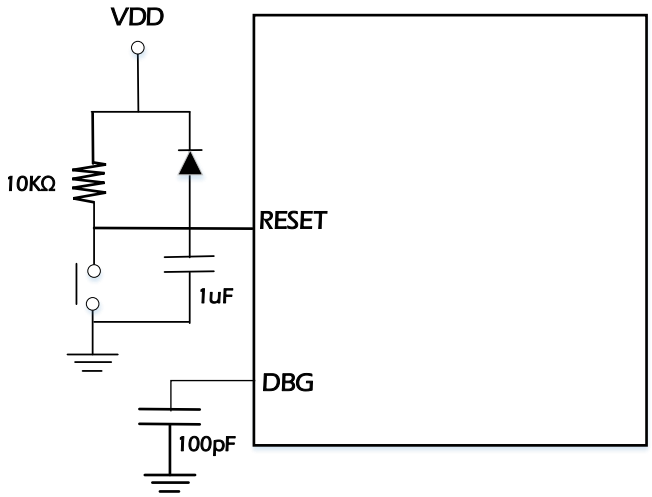


3. Power Decoupling：

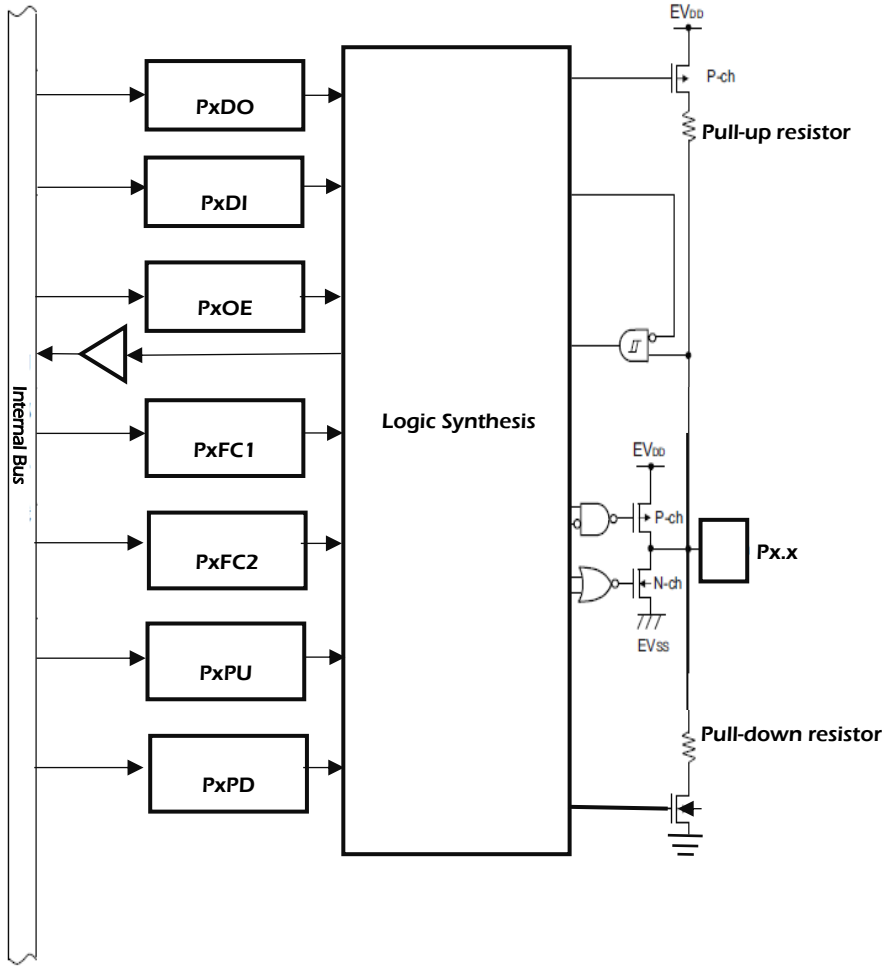


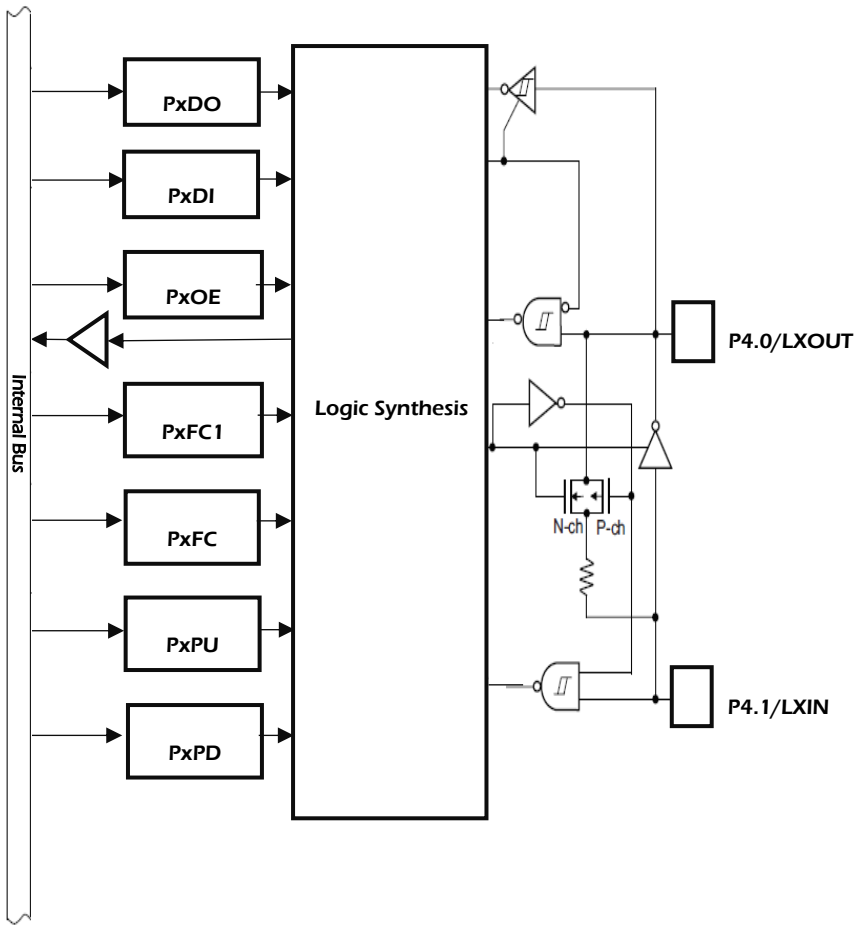
Note： The0.1uF near the VDD should be as close as possible to the IC

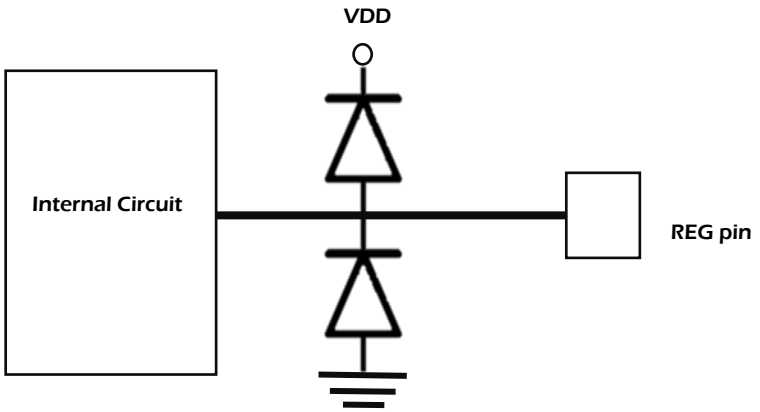
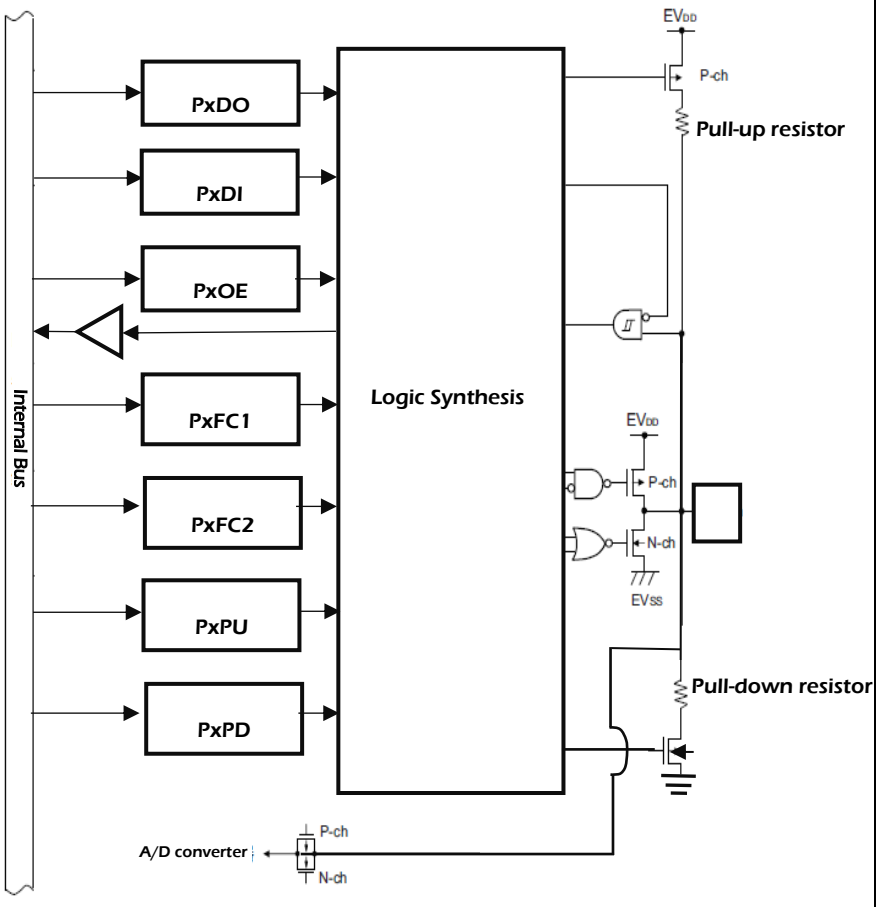
4. RESET and DBG pin：



1.5 I/O Circuit Type

I/O Type	I/O Circuit	Description
Type A		GPIO(withoutADC input) DBG RESET

I/O Type	I/O Circuit	Description
Type B		Connect to external crystal

I/O Type	I/O Circuit	Description
Type C		REG
Type C		GPIO (with ADC input)

2.Electronic Characteristics

2.1Absolute Maximum Rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

(V_{SS} = 0V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}	–	-0.3 to 4.0	V
Input Voltage	V_{IN}	All I/O pins	-0.3 to VDD+0.3	V
Output Current(total)	I_{OUT}	All I/O pins	100	mA
Storage Temperature	T_{STG}	–	-50 to 125	˚C

2.2 Operation Conditons

The following defines the electrical characteristics of the device when it is operated at voltage and temperature maximum/minimum values. Unless otherwise stated, the standard conditions were determined at "operating temperature 25 ° C and operating voltage VDD = 3.3 V".

2.2.1Operation COnditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	2.0	3.3	3.6	V
Analog Supply Voltage	V_{DDA}	2.0	3.3	3.6	V
Operating Temperature	Ta	-40	25	85	℃

2.2.2 Clock Timing

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External Clock Source						
Low Frequency External Crystal (Note 1)	f_{LXIN}	-	-	32768	-	Hz
High Frequency External Crystal (Note1)	f_{HXIN}	-	1	-	16	MHz
Internal Clock Source						
Low Frequency Internal Oscillator (LIRC)	f_{LIRC}	T_A = 25℃	-25%	32	+ 25%	kHz
Low Power Internal Reference Clock (LPIRC)	f_{LPIRC}	T_A = 25℃	- 1%	1	+ 1%	MHz
		T_A = 0~ 50℃ (Note 2)	- 1%	1	+ 1%	
		T_A = -20~ 70℃ (Note 2)	- 1.5%	1	+ 1.5%	
		T_A = -40~ 85℃	- 3%	1	+ 3%	
High Frequency internal Oscillator (HIRC)	f_{HIRC}	T_A = 25℃	- 1%	16	+ 1%	MHz
		T_A = 0~ 50℃ (Note 2)	- 1%	16	+ 1%	
		T_A = -20~ 70℃ (Note 2)	- 1.5%	16	+ 1.5%	
		T_A = -40~ 85℃	- 3%	16	+ 3%	
PLL	f_{PLL}	T_A = 25℃	(Note 3)	24	(Note 3)	MHz

Note 1：It takes around 2.5ms from high frequency external crystal starts to fully oscillating (high frequency external Crystal is 16MHz, Topr= 25℃). It takes around 1.2 sec from low frequency external crystal starts to fully oscillating (low frequency external crystal is 32KHz, Topr=25℃).

Note 2：The test condition is VDD= 3.3V ±10% .

Note 3：The Accuracy of (f_{PLL}) is ±1%, which is the same as PLL reference clock source (16MHz f_{HXIN} or f_{LPIRC}).

2.2.3 I/O Characteristics

VDD=3.3V ,Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}	-	0	-	0.25 VDD	V
Input high voltage	V_{IH}	-	0.75 VDD	-	VDD	V
Output low voltage	V_{OL_050}	IOL=5 mA	-	-	0.4	V
Output high voltage	V_{OH_015}	IOH=1.5 mA	VDD-0.4	-	-	V
Output low current	I_{OL}	0.1xVDD	2.5	6.7	-	mA
		0.3xVDD	7	15	-	mA
Output high current	I_{OH}	0.9xVDD	1	2.4	-	mA
		0.7xVDD	3	5.8	-	mA
Pull-up resistance	R_{PULLUP}	-	10	20	40	kΩ
Pull-low Resistance	R_{PULLDN}	-	10	20	40	kΩ

2.3 D.C. Characteristics

Operating @ 3.3V, Ta=-40~85°C						
Parameter	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Normal Mode (Code executing from Flash)	I_{DD_N0}	LPIRC is PLL clock source f_{LPIRC}=1MHz,fsysclk=24MHz (PLL)	-	4.5	8	mA
	I_{DD_N1}	System clock is HIRC, f_{HXIN}=0MHz,fsysclk=16 MHz (HIRC)	-	3.6	5.5	mA
	I_{DD_N2}	System clock is LIRC, only LIRC enable, fsysclk=32KHz	-	0.7	1.1	mA
	I_{DD_N3}	System clock is HXTAL fsysclk=16MHz (HXTAL)	-	3.8	5.7	mA
	I_{DD_N4}	System clock is LXTAL fsysclk=32768Hz (LXTAL)	-	0.7	1.1	mA
Sleep Mode (CPU clock is stopped)	I_{DD_SL0}	LPIRC is PLL clock source f_{LPIRC}=1MHz,fsysclk=24MHz (PLL)	-	2.7	4.1	mA
	I_{DD_SL1}	System clock is HIRC, f_{HXIN}=0MHz,fsysclk=16 MHz (HIRC)	-	1.8	2.7	mA
	I_{DD_SL2}	System clock is LIRC, only LIRC enable, fsysclk=32KHz	-	0.7	1.1	mA
	I_{DD_SL3}	System clock is HXTAL fsysclk=16MHz (HXTAL)	-	2.0	3.1	mA
	I_{DD_SL4}	System clock is LXTAL fsysclk=32768Hz (LXTAL)	-	0.7	1.1	mA
Deep Sleep Mode (CPU and RAM are retained)	I_{DD_DS0}	RTC Disable	-	1.0	-	uA
	I_{DD_DS1}	RTC Enable, LXTAL on	-	1.9	-	uA

Operating @ 3.3V, Ta=25°C						
Parameter	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Deep Sleep Mode (CPU and RAM are retained)	I_{DD_DS0}	RTC Disable	0.8	1.0	-	uA
	I_{DD_DS1}	RTC Enable, LXTAL on	1.4	1.9	-	uA

Note : The D.C. characteristics are with security processor underdeep sleep mode. The D.C. characteristics which are with security processor under operation mode, please refer to Appendix C.

2.4 Power-on Reset Characteristics

Ta=-40~85℃

Symbol	Description	Min.	Typ.	Max.	Unit
tPPW	Power-on reset minimum pulse width	1	-	-	ms
tPWUP	Warming-up time after a reset is clear and CPU ready Note1	-	4	-	ms
tVDD	Power supply rise time	0.5	-	5	ms

Note1 : tPWUP does not include BOOTROM code execution time. BOOTROM code execution time is around 50ms.

Note2 : Power-on reset voltage using BROR 1st level.

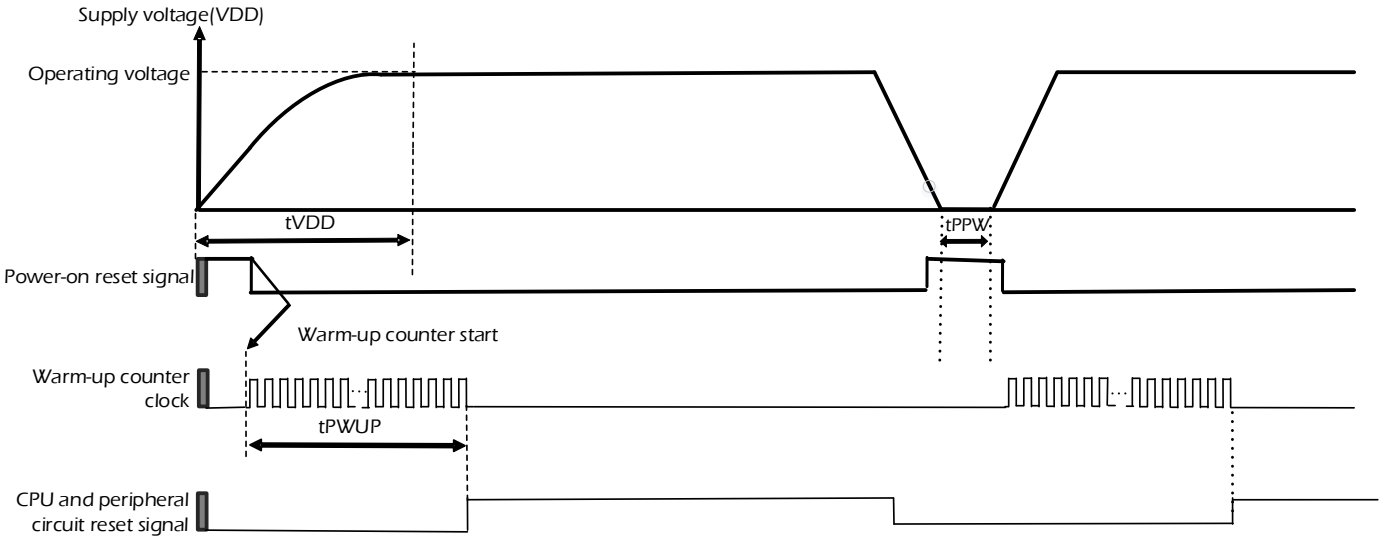


FIGURE2- 1 OPERATION TIMING OF POWER ON RESET

Note：In power-down process, the VDD must be 0 V, then re-power-on to ensure th IC operating normal.

2.5 BROR Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
BROR detected voltage	VBRORON1	BRORCFG=00	1.84	1.90	1.96	V
	VBROROFF1		1.89	1.95	2.01	V
	VBRORON2	BRORCFG=01	2.18	2.25	2.32	V
	VBROROFF2		2.23	2.30	2.37	V
	VBRORON3	BRORCFG=10	2.47	2.55	2.63	V
	VBROROFF3		2.52	2.60	2.68	V
	VBRORON4	BRORCFG=11	2.67	2.75	2.83	V
	VBROROFF4		2.72	2.80	2.88	V

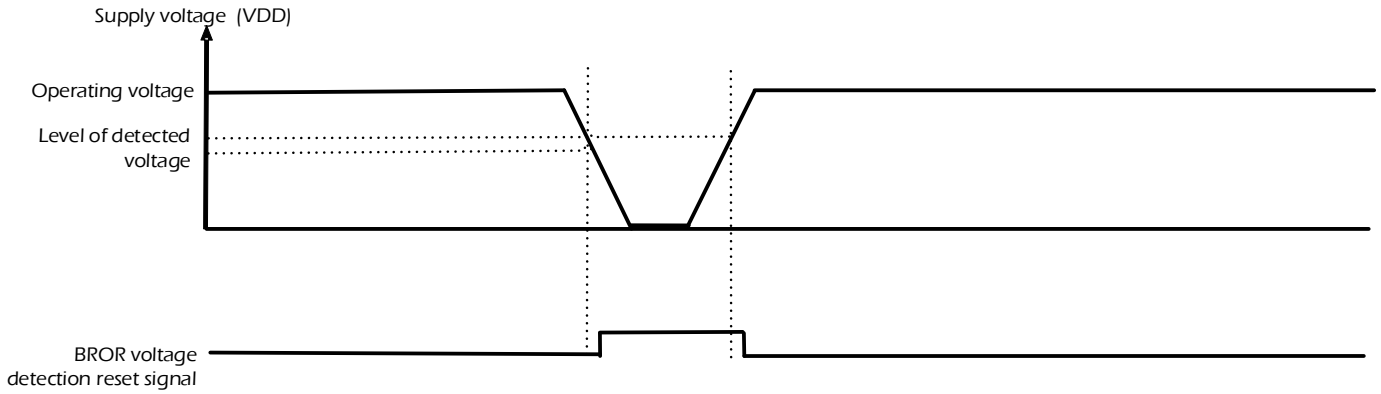


FIGURE 2- 2 BROR

Note：When BROR occurs, do not perform any operation.

2.6 LVD Characteristics

Ta=-40~85℃

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LVD	VLVD1	Falling Mode, LVDCFG=001	2.28	2.35	2.42	V
	VLVD2	Falling Mode, LVDCFG=010	2.57	2.65	2.73	V
	VLVD3	Falling Mode, LVDCFG=011	2.76	2.85	2.94	V
	VLVD4	Falling Mode, LVDCFG=100	3.06	3.15	3.24	V

Parameter	Symbol	Condition	Min.	Typ.	Max.
tVLTON	Voltage detecting detection response time	-	1	10	us

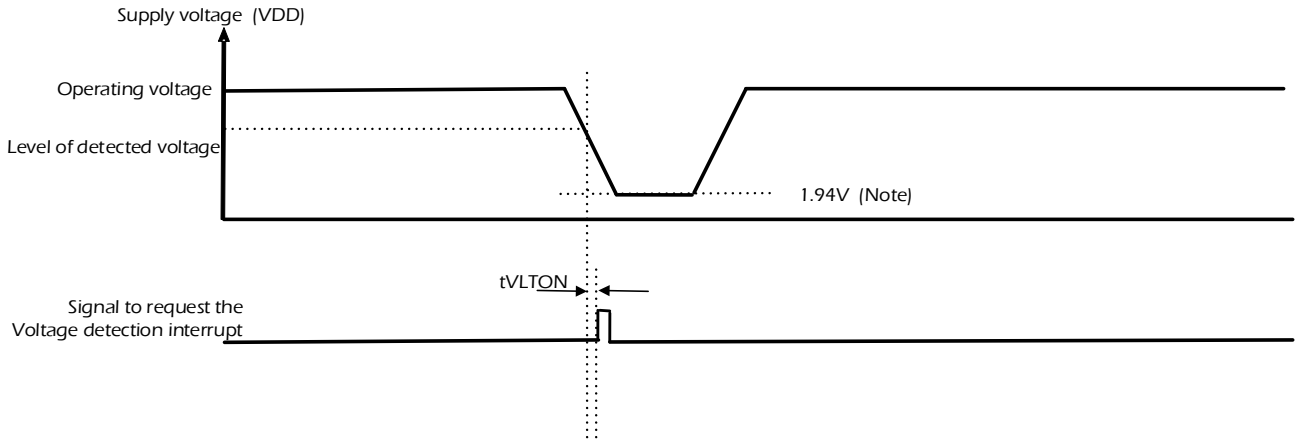


Figure 2- 3 LVD

Note：It may trigger BROR

2.7 ADC Characteristics

VREF_ADC=VDD

2V ≦ VDD ≦ 3.6V, T_A= -45~85℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resolution	RES_{ADC}	-	12	-	bits
Sampling Rate	f_{ADC}	-	-	470	KSPS
Differential Nonlinearity Error (DNL)	DNL_{ADC}	-	-	±4	LSB
Integral Nonlinearity Error (INL)	INL_{ADC}	-	-	±5	LSB
Gain Error	E_{GAIN}	-	-	±6	LSB
Offset Error	E_{OFFSET}	-	-	±6	LSB
Input Voltage Range	V_{ADC_RNG}	-	-	VDD	V
VREF_ADC Voltage Range	V_{REF_ADC}	VDD Note			V
Note：VREF_ADC=VDD, the voltage range 2~3.6V					

Note : ADC sample rate= $\frac{1}{22}$ x $\frac{fsysclk}{\text{ADCCKDIV}}$

When system clock is 24MHz, and setting ADCCKDIV to 0x02, ADC Sample rate : $\frac{1}{22} x \frac{24\text{MHz}}{2^2} = 272.727ksps$

2.8 Flash Characteristics

(V_{SS} = 0V, 2.0V ≦ V_{DD}≦ 3.6V, T_{OPR} = -40 to 85°C)

Parameter	Condition	Min.	Typ.	Max.	Unit
Number of guaranteed writes to flash memory	-	--	--	100,000	times
Flash memory write time	Write Time (per byte)	--	--	7.5	μs
Flashmemory erase time	Chip Erase	--	--	40	ms
	Sector Erase (1 Sector = 512 bytes)	--	--	5	

3. Addressing Space

The address space is divided into program and data spaces. The code and data access can be byte access or word access. The addressable memory space is 64KB of program and 64KB of data memory.

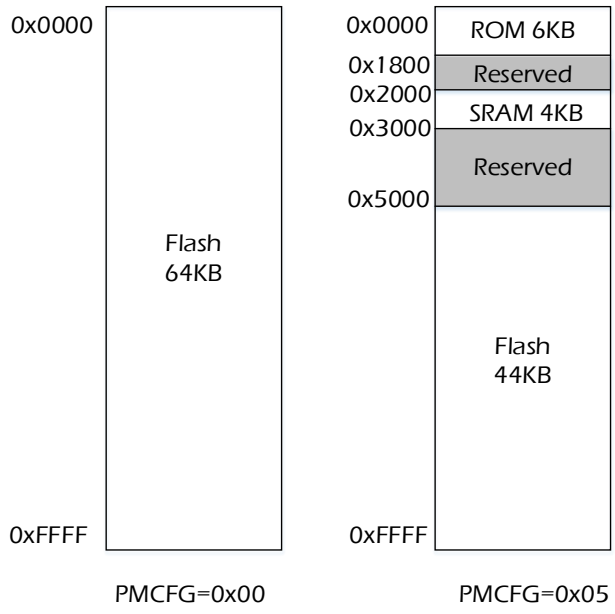


FIGURE 3- 1 PROGRAM MEMORY MAPPING

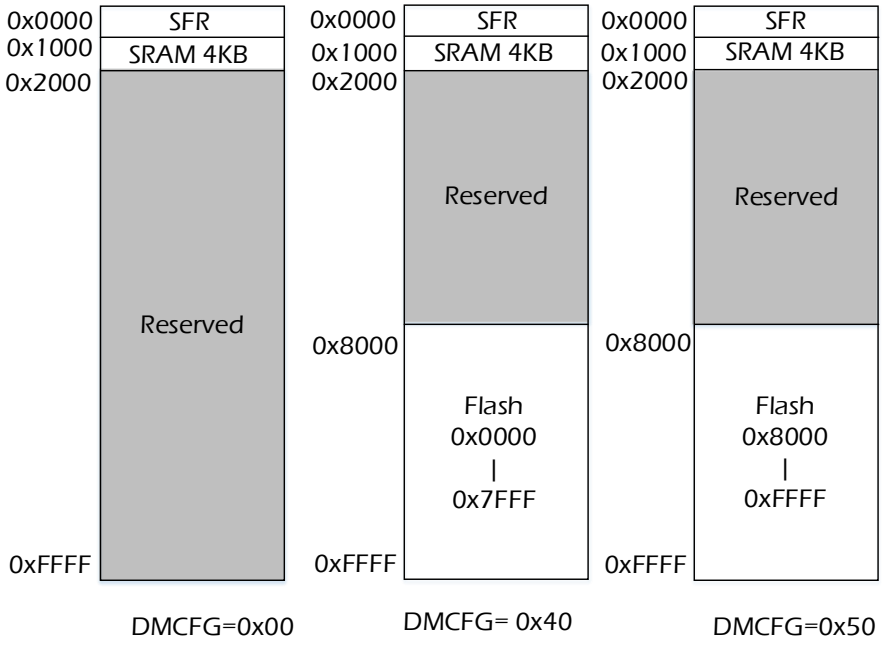


FIGURE 3- 2 DATA MEMORY MAPPING

4. Syetm Operation

4.1 Operating Modes

This device offers three operating modes: Normal mode, Sleep mode , and Deep sleep mode.

Normal mode is the normal operating condition. Enter either Sleep mode or Deep sleep mode, it can reduce the power dissipation. The power consumption under deep sleep mode is 1.9 uA. This table summarizes the functions that are enabled/ disable under different operating modes.

Mode	Normal	Sleep	Deep Sleep
CPU Clock	ON	OFF	OFF
Periph Clock	ON*	ON*	OFF*
LDO	ON	ON	OFF
BROR	ON*	ON*	ON*
LVD	OFF*	OFF*	OFF*
PLL	OFF*	OFF*	OFF
HXTAL	OFF*	OFF*	OFF
LXTAL	OFF*	OFF*	OFF*
HIRC	ON*	ON*	OFF
LIRC	ON	ON	ON
RTC	OFF*	OFF*	OFF*
Flash	ON	ON	OFF
RAM	ON	ON	Retention
Note	*：User can enable or disable by software setting. Retention: Data retention		

TABLE 4- 1 SYSTEM OPERATION MODES

5 Security Processor

Security Processor offers 128-bit TRNG (True Random Number Generator), hardware AES crypto engine and hardware SHA algorithm. There are secure space (Key, User Zone, Small Zone) for key and sensitive data storage.

Note: The detail of SQ7515 Security Processor commands please refer to "SQ7515 Security Processor characteristics and commands"。This document will be provided after NDA complete.

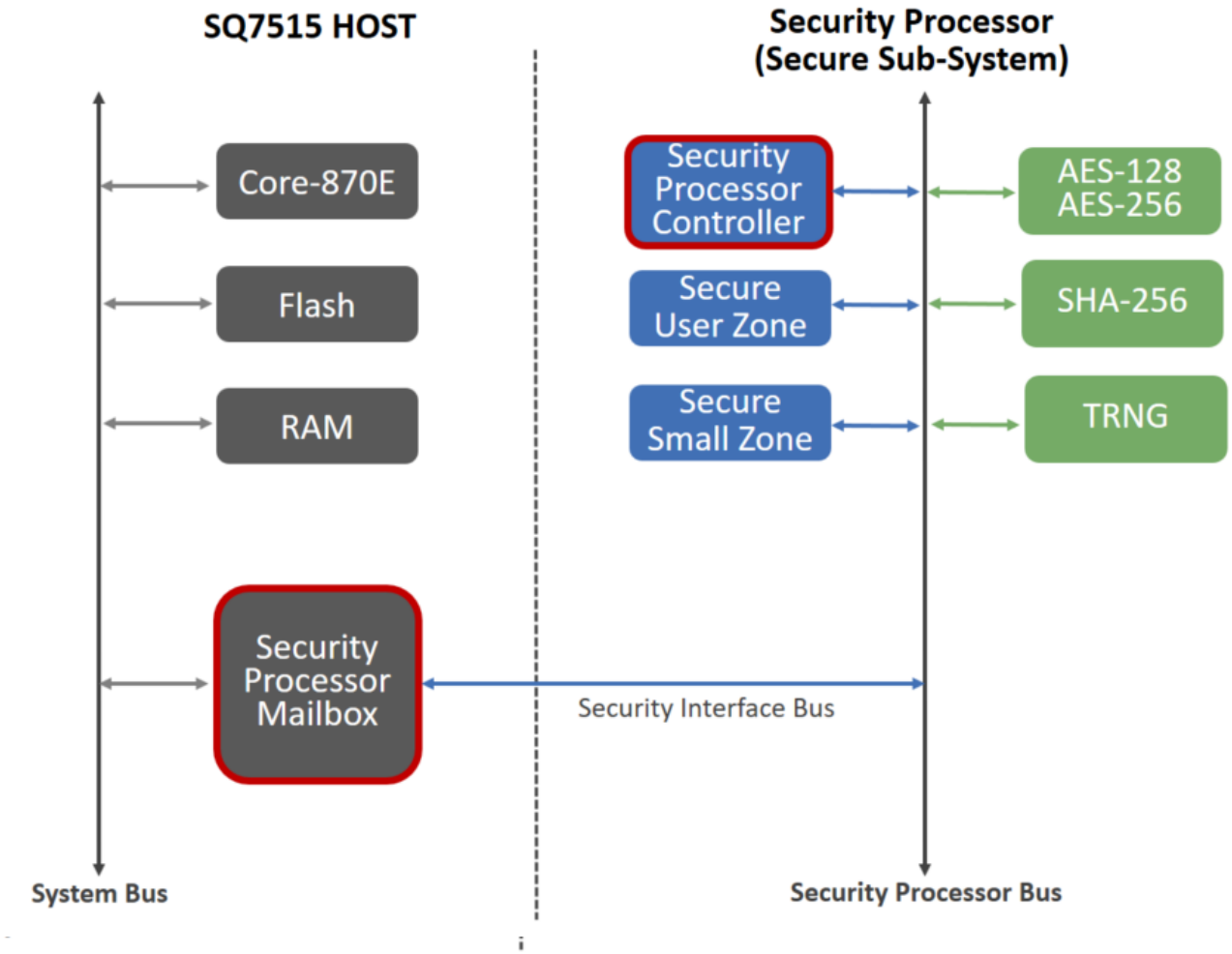


FIGURE 5-1 SECURITY PROCESSOR

Appendix A. Product Number Information

Example： SQ 75 15 QA 044 S E T R

SQ Series

Product Series

Sub Series

Package Type

Code	Package Type	Code	Package Type
ST	SOT23	SD	SDIP
SP	SOP	LQ	LQFP 7x7
MS	MSOP	LA	LQFP 10x10
SS	SSOP	LE	LQFP 14x14
DP	PDIP	N4	QFN 4x4
TS	TSOP	N5	QFN 5x5
DS	TSSOP	QA	QFP 10x10

Pin Count

Code	Pin Count	Code	Pin Count
005	5	032	32
006	6	036	36
008	8	040	40
010	10	044	44
014	14	048	48
016	16	064	64
020	20	080	80
024	24	096	96
028	28	100	100

Program Flash

Data Flash

RAM

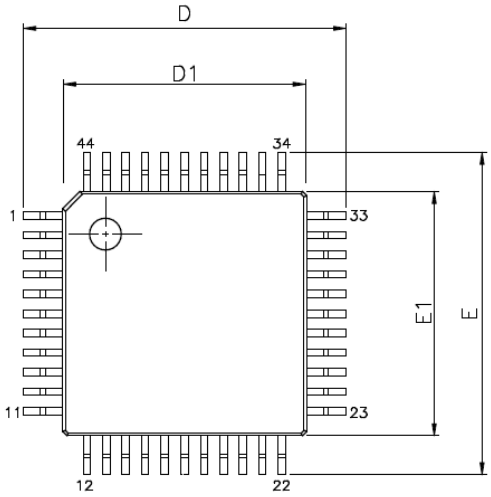
Code	Program Flash/ Data Flash / RAM Size	Code	Program Flash/ Data Flash / RAM Size
A	128 Bytes	K	24K Bytes
B	256 Bytes	M	32K Bytes
E	512 Bytes	N	40K Bytes
J	1K Bytes	P	48K Bytes
L	2K Bytes	S	64K Bytes
T	4K Bytes	U	96K Bytes
G	8K Bytes	W	128K Bytes
C	12K Bytes	V	无
H	16K Bytes		

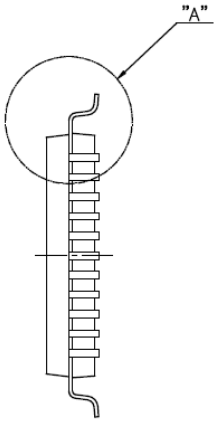
Operating Temp

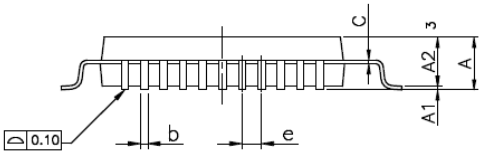
Code	Operating Temp
R	-40~85°C

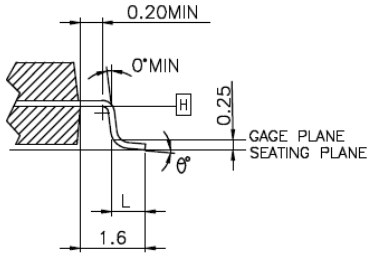
Appendix B. Package Information

QFP44 10x10 (SQ7515QA044SETR)









DETAIL A

	MILLMETER		
	MIN	NOM	MAX
A	–	–	2.70
A1	0.25	–	0.50
A2	1.80	2.00	2.20
b	0.25	0.30	0.35
D	13.00	13.20	13.40
D1	9.90	10.00	10.10
E	–	13.20	–
E1	–	10.00	–
e	0.8 BSC.		
L	0.73	–	0.93
θ	0	–	10°
C	–	0.15	–

Appendix C. Application Note

(A) DC character related

1 The D.C. characters when security processor under operation and deep sleep mode.

Operating @ 3.3V, Ta=25℃				
Parameter	**Symbol**	**Condition**	**Typ.**	**Unit**
Normal Mode (Code executing from Flash) Security Processor under Deep Sleep Mode	I_{DD_N0}	LPIRC is PLL clock source, f_{LPIRC}=1MHz,fsysclk=24MHz,(PLL), Security Processor under Deep Sleep Mode	4.5	mA
	I_{DD_N1}	System clock is HIRC f_{HXIN}=0MHz,fsysclk=16 MHz Security Processor under Deep Sleep Mode	3.6	mA
	I_{DD_N3}	System clock is HXTAL. fsysclk=16MHz), Security Processor under Deep Sleep Mode	3.8	mA
Normal Mode (Code executing from Flash) Security Processor under Operation Mode	$I_{DD\_N0\_SPON}$	LPIRC is PLL clock source, f_{LPIRC}=1MHz,fsysclk=24MHz,(PLL), Security Processor under Operation Mode	9.5	mA
	$I_{DD\_N0\_SPON\_AES}$	LPIRC is PLL clock source, f_{LPIRC}=1MHz,fsysclk=24MHz,(PLL), Security Processor under Operation Mode, AES enable	11	mA
	$I_{DD\_N0\_SPON\_SHA}$	LPIRC is PLL clock source, f_{LPIRC}=1MHz,fsysclk=24MHz,(PLL), Security Processor under Operation Mode, SHA enable	12.5	mA
	$I_{DD\_N0\_SPON\_TRNG}$	LPIRC is PLL clock source, f_{LPIRC}=1MHz,fsysclk=24MHz,(PLL), Security Processor under Operation Mode, TRNG enable	12.5	mA
	$I_{DD\_N1\_SPON}$	System clock is HIRC, fHXIN=0MHz,fsysclk=16 MHz Security Processor under Operation Mode	8.6	mA
	$I_{DD\_N3\ SPON}$	System clock is HXTAL. fsysclk=16MHz), Security Processor under Operation Mode	8.8	mA

Revision History

Version	Approved Date	Description
V1.0	2022/11/7	1ST issued.